UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,355	12/22/2003	Jang-Seok Choi	SAM-0503	9333

7590 01/21/2005

Steven M. Mills
MILLS & ONELLO LLP
Eleven Beacon Street, Suite 605
Boston, MA 02108

EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/743,355	CHOI ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4 and 11-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Borchers et al. (US 2004/0044934).

As to claim 1, Borchers et al.'s figure shows a control signal generation circuit comprising: an input terminal (input of flip-flop 7); a first output terminal (output of flip flop 9); and a second output terminal (output of MUX 13), wherein the control signal generation circuit receives, in response to a clock signal (3), an input signal (4) inputted to the input terminal and outputs a column latch signal and a data input/output command signal, which are separately activated and have a first time interval therebetween, to the first output terminal and the second output terminal, respectively, each in response to a test enable signal (output 14 of circuit 5) at a first state, or outputs the column latch signal and the data input/output command signal, which are separately activated and have a second time interval therebetween, to the first output terminal and the second output terminal, respectively, each in response to a test enable signal at a second state, wherein the first time interval and the second time interval are controlled in units of bit time of the clock signal, and the second time interval is controlled to be smaller than the first

time interval (it is seen as an intended use because the circuit 5 is capable of providing the second time interval to be smaller than the first time interval).

As to claim 2, the figure shows that the first time interval and the second time interval each amount to a time from when the column latch signal is activated to when the data input/output command signal is activated.

As to claim 3, the figure shows a control signal generation circuit comprising: a first latch (7) which latches an input signal (4) in response to a clock signal (3); a second latch (8) which latches an output signal of the first latch in response to the clock signal; a selection circuit (13) which outputs the output signal of the first latch or an output signal of the second latch as a column latch signal in response to a test enable signal (14); and a third latch (9) which latches the output signal of the second latch as a data input/output command signal in response to the clock signal, wherein the amount of time from when the column latch signal is activated to when the data input/output command signal is activated is controlled in units of bit time of the clock signal.

As to claim 4, the figure shows that the input signal is generated by decoding a data write/read command signal and is activated in response to the data write/read command signal (circuit 2 is a memory circuit, it is seen as an intended use to provide write/read command signal as the input of the flip flop 7).

Claims 11 and 12 recite a method with the similar limitations of the claims above. Therefore, they are rejected for the same reasons.

3. Claims 7 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Moloney et al. (USP 5528237).

As to claim 7, Moloney et al.'s figure 5 shows a control signal generation circuit comprising: a first latch (flip flop C) which latches an input signal (Z) in response to a clock signal (output of VCO); a second latch (flip-flop in DD that generates signal ND0') which latches an output signal of the first latch in response to the clock signal; a third latch (the flip flop that generates signal ND0'') which latches an output signal of the second latch in response to the clock signal; and a selection circuit (2-1 MUX) which outputs one of the output signal of the second latch and an output signal of the third latch in response to a test enable signal (VCO/3), wherein the amount of time from when the output signal of the first latch is activated to when an output signal of the selection circuit is activated is controlled in units of bit time of the clock signal.

As to claim 9, it is seen as an intended use to select the output signal of the first latch to be a column latch signal, and the output signal of the selection circuit to a data input/output command signal.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Borchers et al. (US 2004/0044934) in view of Kubota et al. (USP 5654658).

As to claim 5, the figure of Bosrchers et al.'s fails to shows the detail of each flip flop circuit. However, Borchers et al.'s figure 15a shows a flip-flop circuit that is capable of

operating at a high operation speed. Therefore, it would have been obvious to one having ordinary skill in the art to use Kubota et al.'s flip flop for Borchers et al.'s flip flops for the circuit of improving the operation of the circuit. Thus, the circuits which each comprising Kubota et al.'s elements 3, 5, 7 and 8 in the modified flip flops are the claimed first, second and third latch circuits. The modified Bosrchers et al.'s figure further shows a first inverter (Kubota et al.'s inverter 5 in the first modified flip flop) which is connected between an output terminal of the first latch and a first input terminal of the selection circuit; a second inverter (Kubota et al.'s inverter 1 in the modified Borsrchers et al.'s second flip flop) which is connected between the output terminal of the first latch and an input terminal of the second latch; and a third inverter (Kubota et al.'s inverter 6 in the modified second flip flop) which is connected between the output terminal of the second latch and an input terminal of the third latch, wherein the output terminal of the second latch is connected to a second input terminal of the selection circuit.

As to claim 6, the modified Bosrchers et al.'s figure shows the output signal of the first latch (output of Kubota et al.'s inverter 5) is an inverted signal of the input signal.

6. Claims 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moloney et al. (USP 5528237) in view of Kubota et al. (USP 5654658).

As to claim 8, Moloney et al. fails to shows the detail of each flip flop circuit. However, Borchers et al.'s figure 15a shows a flip-flop circuit that is capable of operating at a high operation speed. Therefore, it would have been obvious to one having ordinary skill in the art to use Kubota et al.'s flip flop for Moloney et al.'s flip flops for the circuit of improving the operation of the circuit. Thus, the circuits which each comprising Kubota et al.'s elements 3, 7 and 8 in the modified flip flops are the claimed first, second and third latch circuits, and the

output of Kubota et al.'s inverter 1 is the claimed input signal. The modified Moloney et al. further shows a first inverter (Kubota et al.'s inverter 5 in the modified first flip flop) which inverts the output signal of the first latch; a second inverter (Kubota et al.'s inverter 6 in the modified first flip flop) which is connected between an output terminal of the first latch and an input terminal of the second latch; and a third inverter (Kubota et al.'s inverter 6 in the modified second inverter) which is connected between an output terminal of the second latch and an input terminal of the third latch, wherein the selection circuit has a first input terminal connected to an output terminal of the third latch and a second input terminal connected to the output terminal of the second latch.

As to claim 10, the modified Borchers et al.'s figure 15a that the output signal of the first latch is an inverted signal of the input signal.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quan Tra
Primary Examiner

January 18, 2005